REMARKS/ARGUMENTS

Favorable consideration of this application in light of the following discussion is respectfully requested.

Claims 1-3 and 5-22 are presently pending in this application, no amendments are made herein.

In the outstanding Office Action, Claims 1-3 and 5-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Azuma (U.S. Patent 6,836,011) in view of Turlik et al. (U.S. Patent 5,325,265), Farooq et al. (U.S. Patent 6,335,210), Ikeda (JP 11-054884), Milkovich et al. (U.S. 6,516,513), Berrett (U.S. 6,452,807) and JP 59-000996 (hereinafter "JP '996"); Claims 11-19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Azuma, Turlik et al., Farooq et al., Ikeda, Milkovich et al. Berrett and JP '996, and further in view of U.S. 6,193,524 to Chang; Claims 2, 5, 9, 12, 14 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Azuma, Turlik et al., Farooq et al., Ikeda, Milkovich et al. and JP '996, and further in view of Uchikawa et al.; and Claim 20 is not specifically rejected.

Applicants first note that the present Response makes no amendment to the claims, and the remarks below clearly explain the distinctions of the claimed invention over the cited references. While Applicants believe that these remarks should result in allowance of the claims in their present form, Applicants respectfully request that the Examiner contact the undersigned to discuss any amendments to the claims that the Examiner may deem necessary to clarify the distinctions discussed below and place this case in condition for allowance. Alternatively, Applicants respectfully request that the any forthcoming Office Action address each of the distinctions detailed below in order to fully develop these issues so that suitability of an Appeal in this case can be determined. Finally, as no amendments are made herein, any

new ground of rejection in a forthcoming Office Action will not be necessitated by amendment and cannot be properly made final.[1]

Turning now to the merits, Applicants' invention is directed to an interposer that can be provided between a package substrate and an IC chip electrically connected to the package substrate. As discussed in the Background section of Applicants' specification, high frequency IC chips are typically made of a brittle porous material that is prone to cracking under thermal stress. Thus, stress defects in the IC chip occur during loading of the substrate with the IC.[2] Applicants' invention is directed to addressing this problem.

Specifically, Applicants' Claim 1 recites an interposer configured to be located between a package substrate made of resin and an IC chip. The interposer includes an insulating base material, wherein a Young's modulus of the insulation base material is 55 to 440GPa and a thickness of the insulation base material is 0.05 to 1.5 times the thickness of the package substrate. Also recited is a plurality of through holes provided through the insulating base material, each of the plurality of through holes having a diameter of 125 μm or less and having formed therein a through hole conductor for connecting the package substrate with the IC chip, wherein the plurality of through holes in the insulating base material are arranged in the form of a grid. Claim 11 recites similar features except that plurality of through holes in the insulating base material are arranged in to be staggered.

Thus, Applicants Claims 1 and 11 recite that a

> Young's modulus of insulation base material is 55 to 440Gpa and ***a thickness of the insulating base material is 0.05 to 1.5 times the thickness of the package substrate.***

As discussed on record in this case, the cited combination of Azuma, Turlik et al., Farooq et al., Ikeda, Milkovich et al., Berrett and JP '996 (and nor does Chang and Uchikawa et al.)

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[1] MPEP 706.07(a)
[2] US Patent Publication No. 2006/0202322 (Applicants specification) at paragraph 4.

does not disclose that the "thickness of the insulating base material is 0.05 to 1.5 times the thickness of the package substrate." The Office Actions acknowledge that the claimed thickness range is not disclosed in the cited references, but conclude that this feature is depicted in the drawings or obvious to one skilled in the art due to design and manufacturing considerations. However, none of the cited references disclose anything about thickness values of the interposer in relation to the package substrate, and none of the cited references disclose scaled drawings by which one could measure and calculate the thickness range based solely on the drawings. Applicants submit that the Office Actions provide only general assertions that the thickness range "is too broad" or fall within "normal production" techniques, which cannot support a finding that the cited references disclose that the "thickness of the insulating base material is 0.05 to 1.5 times the thickness of the package substrate," as required by Claims 1 and 11.

Even assuming that the claimed thickness range is found in the prior art, one of ordinary skill in the art would not combine the claimed interposer thickness range with the claimed Young's modulus range to arrive at Applicants' invention. Specifically, it is the present inventors who analyzed thermal stress during loading of the IC onto the substrate under various conditions and discovered a particular advantage to combining the claimed Young's modulus and thickness.[3] That is, the inventors discovered that the combined features of the claimed Young's modulus and the claimed thickness range provide an improved configuration that suppresses deformation of the insulation base material and crevice or breaking in the resin layer of the IC. None of the seven references combined for rejecting Claims 1 and 11 disclose any importance of the thickness relationship of an interposer to a package substrate, let alone this relationship in combination with the claimed

[3] Applicants' specification at paragraph 24.

thickness range. In view of this, Applicants submit that combination of these features is impermissible hindsight reasoning based on Applicants' disclosure.

Thus, the cited references do not disclose or render obvious the feature of a Young's modulus of insulation base material is 55 to 440Gpa ***and*** a thickness of the insulating base material is 0.05 to 1.5 times the thickness of the package substrate. This alone provides reason for allowance of Claims 1 and 11.

Nevertheless, Applicants' Claims 1 and 11 also recite,

> ***each of the plurality of through holes having a diameter of 125 μm or less*** and having formed therein a through hole conductor for connecting said package substrate with the IC chip.

As discussed in Applicants' specification, when the diameter of the through hole is 125 μm or less, the amount of heat generation increases in the through holes because conductor resistance increases. The claimed invention is directed to this particular situation in which a small diameter through hole (125 μm or less) generates excessive heat.

None of the references in the cited combination of Azuma, Turlik et al., Farooq et al., Ikeda, Milkovich et al., Berrett and JP '996 (and nor does Chang and Uchikawa et al.) disclose the feature of the plurality of through holes having a diameter of 125 μm or less. That is, none of the cited references disclose the claimed feature which causes the reliability problems discussed in the specification and addressed by the claimed invention. In this regard, Applicants note that the outstanding Office Action does not cite any references as teaching this feature, but rather takes the position that the limitation of a diameter of 125 μm or less "is seen to be a matter of typical engineering design." However, the Office Action does not provide a plausible reason why one of ordinary skill in the art would limit a design of the interposer to this diameter size through hole. Thus, through holes having a diameter of 125 μm or less provides another patentable distinction of the claimed invention over the cited references.

Moreover, the claimed through hole size is not claimed in isolation, but rather in combination with the inventive solution that mitigates problems that arises from the small diameter size feature. That is, if one skilled in the art chose to design an interposer having through holes with the recited small diameter, then the resulting interposer would have the problems that Applicants specification discusses in the Background. But Applicants' Claims 1 and 11 also recite,

> Claim 1... wherein the plurality of through holes in the insulating base material are arranged ***in the form of a grid.***
> Claim 11... wherein the plurality of through holes in the insulating base material are arranged ***in the form of a staggered arrangement.***

As noted above, when the diameter of the through hole is small, the amount of heat generation increases in the through holes because conductor resistance increases. Where the through holes are disposed in the form of the grid (as in Claim 1) or in the staggered fashion (as in Claim 11), "the temperature distribution of the interposer at the time of usage becomes uniform so that no stress concentrates on any specific location thereby the insulation layer of the IC chip being not damaged. Further, the physical property (thermal expansion coefficient, Young's modulus and the like) of the insulation base material just below the IC chip becomes uniform because the through holes are formed uniformly."[4] None of the cited references disclose this additional feature of the through holes being in a grid or staggered arrangement. This provides an additional basis for patentability of independent Claims 1 and 11 over the cited references.

For the reasons discussed above, Claims 1 and 11 patentably define over the cited references. Further, as the remaining pending claims depend from Claims 1 or 11, these claims also patentably define over the cited references.

[4] Applicants' specification at paragraph 23.

Nevertheless, dependent Claims 8 and 17 recite that the diameter of an opening in at least an end face of the through hole is equal to or larger than the diameter of the hole in the center of the through hole. As discussed in Applicants' specification, this feature provides advantages of reducing heat and thermal stress in the area of the through hole.[5] Further, Claims 20 and 21 specify that the a set of said plurality of through holes corresponding to either a power source electrode or ground electrode terminal of the IC chip are arranged in said grid to effect substantially uniform temperature of the interposer. Similarly, Claim 22 recites that the plurality of through holes are arranged at substantially equal distance from each other. As discussed in Applicant's specification, these features further reduce thermal stress on the interposer.[6] None of the cited references disclose these features, and thus, the above dependent claims provide addition bases for patentability over the cited references.

Consequently, in view of the remarks above, no further issues are believed to be outstanding in the present application and the present application is believed to be in condition for allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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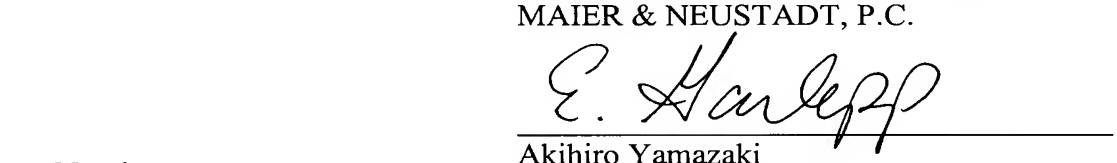

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[5] Applicants' specification at paragraph 24.
[6] Applicants' specification at paragraph 23.